What is claimed is:

1. A frequency comparator circuit, comprising:

a detector circuit that is configured to provide first and second reset signals from first and second input signals such that:

if a first frequency that is associated with the first input signal is greater than a second frequency that is associated with the second input signal, the first reset signal includes a first parameter that is related to a difference between the first and second frequencies, and

if the first frequency is less than the second frequency, the second reset signal includes a second parameter that is related to the difference between the first and second frequencies; and

a tolerance circuit that is arranged to provide a status signal from the first and second input signals and the first and second reset signals such that the status signal corresponds to:

a first logic level, if the difference between the first and second frequencies is within a tolerance window; and

a second logic level, if the difference between the first and second frequencies is outside of the tolerance window.

2. The frequency comparator circuit of Claim 1, wherein the first parameter includes at least one of a frequency of the first reset signal and a duty cycle of the first reset signal.

3. The frequency comparator circuit of Claim 1, wherein the second parameter includes at least one of a frequency of the second reset signal and a duty cycle of the second reset signal.

4. The frequency comparator circuit of Claim 1, wherein the first parameter includes a frequency of the first reset signal if the first frequency is relatively close to the second frequency.

5. The frequency comparator circuit of Claim 1, wherein the second parameter includes the frequency of the second reset signal if the second frequency is relatively close to the first frequency.

6. The frequency comparator circuit of Claim 1, wherein the detector circuit is a frequency detector circuit, wherein the frequency detector circuit is arranged such that the first and second reset signals are substantially independent of the phases of the first and second input signals.

7. The frequency comparator circuit of Claim 1, wherein the detector circuit includes four flip-flops and a clear logic circuit.

8. The frequency comparator circuit of Claim 1, wherein the detector circuit includes:

a clear logic circuit that is arranged to activate a clear signal if a first intermediate signal and a second intermediate signal correspond to the first logic level, and arranged to deactivate the clear signal if at least one of the first intermediate signal and the second intermediate signal corresponds to the second logic level;

a first flip-flop circuit that is arranged to set the first intermediate signal to the first logic level in response to the first input signal if the clear signal is deactivated, and arranged to reset the first intermediate signal to the second logic level if the clear signal is activated;

a second flip-flop circuit that is arranged to set the second intermediate signal to the first logic level in response to the second input signal if the clear signal is deactivated, and arranged to reset the second intermediate signal to the second logic level if the clear signal is activated;

a third flip-flop circuit that is arranged to activate the first reset signal in response to the first input signal if the first intermediate signal corresponds to the first logic level, such that the first reset signal is activated if the first input signal pulses twice before the clear signal is activated; and

a fourth flip-flop circuit that is arranged to activate the second reset signal in response to the second input signal if the second intermediate signal corresponds to the first logic level, such that the second reset signal is activated if the second input signal pulses twice before the clear signal is activated, wherein the first and second reset signals are related to the difference in frequencies between the first input signal and the second-input signal.

9. The frequency comparator circuit of Claim 1, wherein the tolerance circuit includes:

a first counter circuit that is configured to generate a first count from the first input signal, to reset the first count if the first reset signal corresponds to an asserted logic level, and to provide a first overflow signal such that the first overflow signal is asserted if a first overflow condition has occurred, wherein the first overflow condition is related to the first count; and

a second counter circuit that is configured to generate a second count from the second input signal, to reset the second count if the second reset signal corresponds to an asserted logic level, and to provide a second overflow signal such that the second overflow signal is asserted if a second overflow condition has occurred, wherein the second overflow condition is related to the second count.

10. The frequency comparator circuit of Claim 9, further comprising:

a logic circuit that is configured to provide a status signal such that the status signal corresponds to:

an asserted logic level, if the first and second overflow signals are both asserted, and

a de-asserted logic level, if less than both of the first and second overflow signals are asserted.

11. The frequency comparator circuit of Claim 9, wherein the first counter circuit is configured to store the first overflow condition, and wherein the second counter circuit is configured to store the second overflow condition.

12. A frequency comparator circuit, comprising:

a frequency detector circuit having at least first and second inputs, and first and second outputs;

a first counter circuit having at least a clock input that is coupled to the first input of the frequency detector circuit, and a clear input that is coupled to the first input of the frequency detector circuit;

a second counter circuit having at least a clock input that is coupled to the second input of the frequency detector circuit, and a clear input that is coupled to the second input of the frequency detector circuit.

13. The frequency comparator circuit of Claim 12, further comprising an AND circuit that is coupled to the first and second counter circuits.

14. The frequency comparator circuit of Claim 12, further comprising an AND gate having a first input that is coupled to an overflow output of the first counter circuit, and a second input that is coupled to an overflow output of the second counter circuit.

15. The frequency comparator circuit of Claim 12, wherein the frequency detector circuit is configured to receive first and second input signals at the first and second inputs, a first frequency is associated with the first input signal, a second frequency is associated with a second input signal, and wherein the frequency detector circuit is further configured to provide first and second reset signals at the first and second outputs such that, if the first and second frequencies are relatively close:

if the first frequency is greater than the second frequency, the first reset signal includes a first parameter that is related to a difference between the first and second frequencies, and

if the first frequency is less than the second frequency, the second reset signal includes a second parameter that is related to the difference between the first and second frequencies.

16. The frequency comparator circuit of Claim 12, wherein the frequency detector circuit includes four flip-flops and a clear logic circuit.

17. The frequency comparator circuit of Claim 12, wherein the first counter circuit includes:

a register circuit; and

a flip-flop that is arranged to store an overflow condition related to the register circuit, and

wherein the frequency comparator circuit further includes a delay circuit that is coupled between the clock input of the frequency detector circuit and the clock input of the register circuit.

18. The frequency comparator circuit of Claim 12, wherein the frequency detector circuit includes:

a first flip-flop circuit having a clock input that is coupled to the clock input of the first counter circuit;

a second flip-flop circuit having a clock input that is coupled to the clock input of the second counter circuit;

a third flip-flop circuit having a clock input that is coupled to the clock input of the first counter circuit, another input that is coupled to an output of the first flip-flop circuit, and an output that is coupled to the clear input of the first counter circuit;

fourth flip-flop circuit having a clock input that is coupled to the clock input of the second counter circuit, another input that is coupled to an output of the second flip-flop circuit, and an output that is coupled to the clear input of the second counter circuit; and

a clear logic circuit having a first input that is coupled to the output of the first flip-flop circuit, a second input that is coupled to the output of the second flip-flop circuit, and an output that is coupled to a clear input of the first flip-flop circuit, and further coupled to a clear input of the second flip-flop circuit.

19. The circuit of Claim 18, wherein the clear logic circuit includes:

a delay circuit;

a NAND logic circuit that includes an input that is coupled to the output of the first flip-flop circuit, another input that is coupled to the output of the second flip-flop circuit, and an output that is coupled to an input of the delay circuit; and

an inverter circuit that includes an input that is coupled to an output terminal of the delay circuit, and an output that is coupled to the clear input of the first flip-flop circuit.

20. A frequency comparator circuit, comprising:

means for providing first and second reset signals from first and second input signals such that:

if a first frequency that is associated with the first input signal is greater than a second frequency that is associated with the second input signal, the first reset signal includes a first parameter that is related to a difference between the first and second frequencies, and

if the first frequency is less than the second frequency, the second reset signal includes a second parameter that is related to the difference between the first and second frequencies; and

means for providing a status signal from the first and second input signals and the first and second reset signals such that the status signal corresponds to:

a first logic level, if the difference between the first and second frequencies is less than a tolerance value; and

a second logic level, if the difference between the first and second frequencies is greater than the tolerance value.